CLAIMS:

What is claimed is:

1. A method in a data processing system for dynamically selecting software buffers for aggregation in order to optimize system performance, said method comprising:

receiving data to be transferred to a device, said data being stored in a chain of software buffers;

determining current characteristics of said system; and

dynamically selecting ones of said software buffers to combine that will maximize performance of said system while said data is being transferred.

2. The method according to claim 1, further comprising the steps of:

determining current characteristics of said system including determining direct memory access (DMA) capabilities and processor capacity of said system, wherein said DMA capabilities and process capacity are said characteristics.

3. The method according to claim 1, further comprising the steps of:

generating a new chain of buffers that includes an aggregation of said selected ones of said software buffers.

4. The method according to claim 1, further comprising the steps of:

setting a threshold for each combination of I/O adapter, slot size, and system characteristics.

5. The method according to claim 1, further comprising:

determining a threshold that has been assigned to an I/O adapter that is to be used to receive said data;

evaluating a first buffer in said chain;

determining whether said first buffer is larger than said threshold;

in response to a determination that said first buffer is larger than said threshold, leaving said first buffer unchanged; and

in response to a determination that said first buffer is not larger than said threshold, replacing said first and said second buffers said chain with an aggregated buffer which is a combination of said first and said second buffers.

6. The method according to claim 1, further comprising the steps of:

determining a threshold that has been assigned to an I/O adapter that is to be used to receive said data;

evaluating a first buffer in said chain;

determining whether said first buffer is larger than said threshold;

in response to a determination that said first buffer is larger than said threshold, leaving said first buffer unchanged and creating a new chain of buffers that includes said unchanged first buffer; and

in response to a determination that said first buffer is not larger than said threshold, combining said first buffer with a second buffer in said chain to create a new buffer that is a combination of said first buffer and said second buffer, and creating a new chain of buffers that includes said new buffer instead of either said first or said second buffer.

7. The method according to claim 6, further comprising the steps of:

transmitting said data using said new chain instead of said chain.

8. The method according to claim 1, further comprising:

determining whether said system is more limited by its I/O subsystem capacity or its processor capacity;

in response to a determination that said system is more limited by its I/O subsystem capacity, increasing a level of aggregation of said software buffers; and

in response to a determination that said system is more limited by its processor capacity, restricting said level of aggregation of said software buffers.

9. The method according to claim 8, further comprising:

determining whether said system is more limited by its I/O subsystem capacity or its processor capacity by comparing a size of each one of said software buffers to a threshold size.

10. A method data processing system for dynamically selecting software buffers for aggregation in order to optimize system performance, said system comprising:

a device for receiving data to be transferred to said device, said data being stored in a chain of software buffers;

said system including a CPU executing code for determining current characteristics of said system; and

said CPU executing code for dynamically selecting ones of said software buffers to combine that will maximize performance of said system while said data is being transferred.

11. The system according to claim 10, further comprising:

said current characteristics of said system including direct memory access (DMA) capabilities and processor capacity of said system.

12. The system according to claim 10, further comprising:

said CPU executing code for generating a new chain of buffers that includes an aggregation of said selected ones of said software buffers.

13. The system according to claim 10, further comprising:

a threshold set for each combination of I/O adapter, slot size, and system characteristics.

14. The system according to claim 10, further comprising:

a threshold being determined that has been assigned to an I/O adapter that is to be used to receive said data;

a first buffer in said chain;

said CPU executing code for determining whether said first buffer is larger than said threshold;

in response to a determination that said first buffer is larger than said threshold, said first buffer being left unchanged and a new chain of buffers being created that includes said unchanged first buffer; and

in response to a determination that said first buffer is not larger than said threshold, said first buffer being combined with a second buffer in said chain to create a new buffer that is a combination of said first buffer and said second buffer, and a new chain of buffers being created that includes said new buffer instead of either said first or said second buffer.

15. The system according to claim 14, further comprising:

said data being transmitted using said new chain instead of said chain.

16. The system according to claim 10, further comprising:

said CPU executing code for determining whether said system is more limited by its I/O subsystem capacity or its processor capacity;

in response to a determination that said system is more limited by its I/O subsystem capacity, a level of aggregation of said software buffers being increased; and

in response to a determination that said system is more limited by its processor capacity, said level of aggregation of said software buffers being restricted.

17. The system according to claim 16, further comprising:

said CPU executing code for determining whether said system is more limited by its I/O subsystem capacity or its processor capacity by comparing a size of each one of said software buffers to a threshold size.

18. A computer program product for dynamically selecting software buffers for aggregation in order to optimize system performance, said product comprising:

instruction means for receiving data to be transferred to a device, said data being stored in a chain of software buffers;

instruction means for determining current characteristics of said system; and

instruction means for dynamically selecting ones of said software buffers to combine that will maximize performance of said system while said data is being transferred.

19. The product according to claim 18, further comprising:

instruction means for determining a threshold that has been assigned to an I/O adapter that is to be used to receive said data;

instruction means for evaluating a first buffer in said chain;

instruction means for determining whether said first buffer is larger than said threshold;

in response to a determination that said first buffer is larger than said threshold, instruction means for leaving said first buffer unchanged and for creating a new chain of buffers that includes said unchanged first buffer; and

in response to a determination that said first buffer is not larger than said threshold, instruction means for combining said first buffer with a second buffer in said chain to create a new buffer that is a combination of said first buffer and said second buffer, and for creating a new chain of buffers that includes said new buffer instead of either said first or said second buffer.

20. The product according to claim 18, further comprising:

instruction means for determining whether said system is more limited by its I/O subsystem capacity or its processor capacity;

in response to a determination that said system is more limited by its I/O subsystem capacity, instruction means for increasing a level of aggregation of said software buffers; and

in response to a determination that said system is more limited by its processor capacity, instruction means for restricting said level of aggregation of said software buffers.